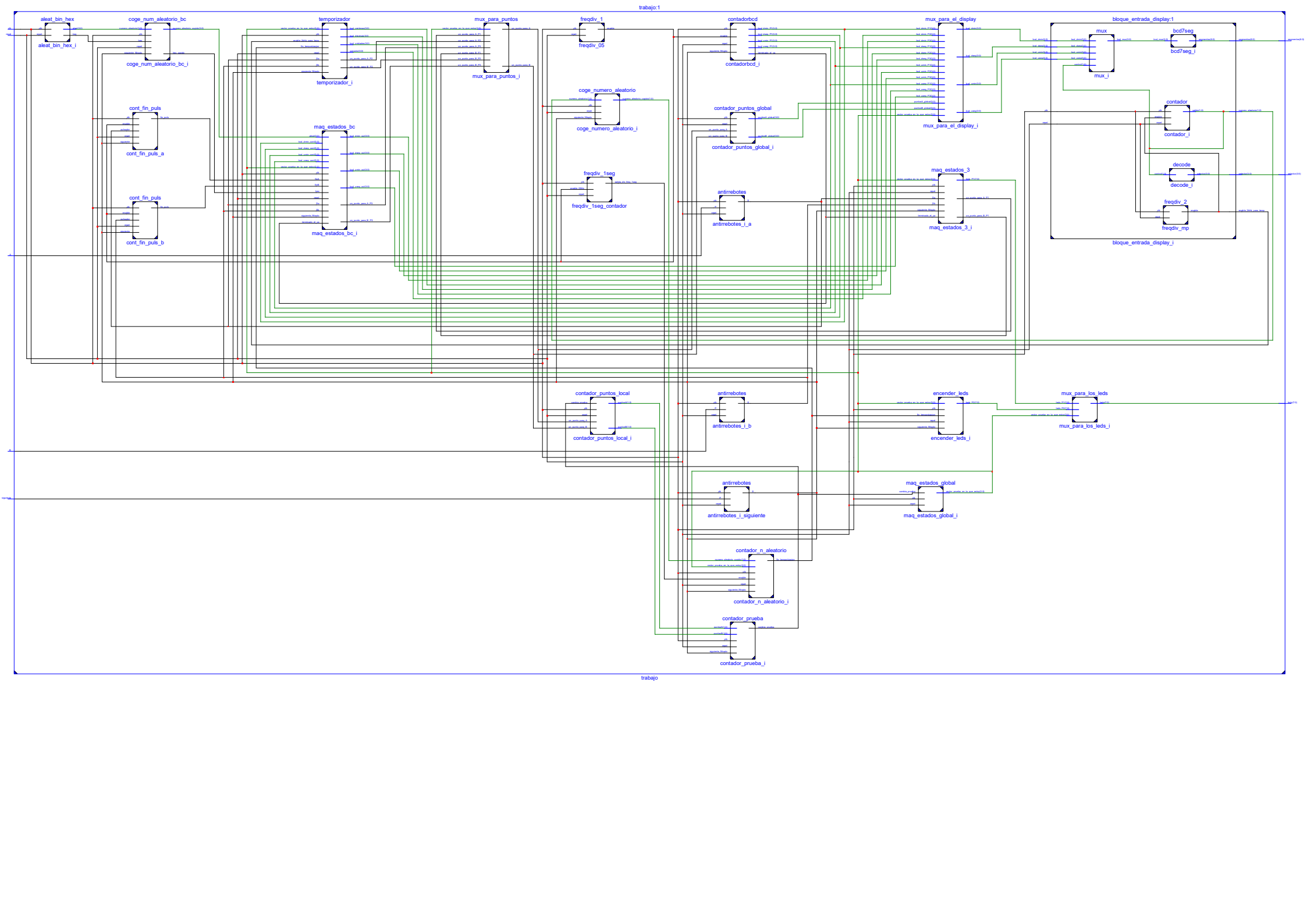
trabajo:1
aleat_bin_hex
aleat_bin_hex_i
coge_num_aleatorio_bc
coge_num_aleatorio_bc_i
temporizador
temporizador_i
mux_para_puntos
mux_para_puntos_i
freqdiv_1
freqdiv_05
contadorbcd
contadorbcd_i
mux_para_el_display
mux_para_el_display_i
bloque_entrada_display:1
mux
mux_i
bcd7seg
bcd7seg_i
contador
contador_i
decode
decode_i
freqdiv_2
freqdiv_mp
bloque_entrada_display_i
cont_fin_puls
cont_fin_puls_a
cont_fin_puls
cont_fin_puls_b
maq_estados_bc
maq_estados_bc_i
coge_numero_aleatorio
coge_numero_aleatorio_i
contador_puntos_global
contador_puntos_global_i
freqdiv_1seg
freqdiv_1seg_contador
antirrebotes
antirrebotes_i_a
maq_estados_3
maq_estados_3_i
contador_puntos_local
contador_puntos_local_i
antirrebotes
antirrebotes_i_b
encender_leds
encender_leds_i
mux_para_los_leds
mux_para_los_leds_i
antirrebotes
antirrebotes_i_siguiente
maq_estados_global
maq_estados_global_i
contador_n_aleatorio
contador_n_aleatorio_i
contador_prueba
contador_prueba_i
trabajo

trabajo Project Status (01/11/2016 - 17:20:26)			
Project File:	mi_proyecto.xise	**Parser Errors:**	No Errors
Module Name:	trabajo	**Implementation State:**	Programming File Generated
Target Device:	xc3s250e-5cp132	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	28 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	190	4,896	3%	
Number of 4 input LUTs	390	4,896	7%	
Number of occupied Slices	265	2,448	10%	
Number of Slices containing only related logic	265	265	100%	
Number of Slices containing unrelated logic	0	265	0%	
Total Number of 4 input LUTs	447	4,896	9%	
Number used as logic	390			
Number used as a route-thru	57			
Number of bonded IOBs	24	92	26%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	3.56			

Performance Summary [-]			
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	lu. 11. ene. 17:12:41 2016	0	28 Warnings (0 new)	8 Infos (0 new)
Translation Report	Current	lu. 11. ene. 17:19:35 2016	0	0	0
Map Report	Current	lu. 11. ene. 17:19:41 2016	0	0	2 Infos (2 new)
Place and Route Report	Current	lu. 11. ene. 17:20:04 2016	0	0	2 Infos (2 new)
Power Report					
Post-PAR Static Timing Report	Current	lu. 11. ene. 17:20:09 2016	0	0	6 Infos (6 new)
Bitgen Report	Current	lu. 11. ene. 17:20:18 2016	0	0	0

Secondary Reports [-]		
Report Name	**Status**	**Generated**
WebTalk Report	Current	lu. 11. ene. 17:20:19 2016
WebTalk Log File	Current	lu. 11. ene. 17:20:26 2016

Date Generated: 01/11/2016 - 17:20:26